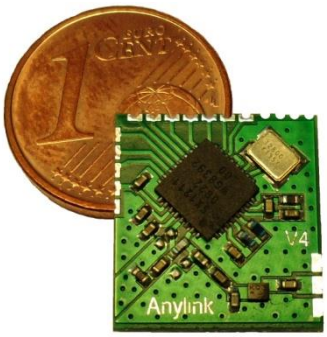

DPS1211 – C868/C915/C950

868, 915 and 950 MHz Drop-In RF Transceiver Modules

Combine Small Form Factor with High Performance

GENERAL DESCRIPTION

The DPS1211 is a low cost transceiver operating in the frequency ranges from 863-870, 902- 928 MHz and 950-960 MHz. The DPS1211 is optimized for very low power consumption (3mA in receive mode). And for very small form factor. It incorporates a baseband modem with data rates up to 200 kb/s. Data handling features include a sixty-four byte FIFO, packet handling, automatic CRC generation and data whitening. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC part 15) regulatory standards.

KEY PRODUCT FEATURES

- Low area needed (15mm x 14mm)
- Low Rx power consumption: 3mA
- Low Tx power consumption: 25 mA @ +10 dBm
- Good reception sensitivity: down to -107 dBm at 25 kb/s in FSK, -113 dBm at 2kb/s in OOK
- Programmable RF output power: up to +12.5 dBm in 8 steps
- Packet handling feature with data whitening and automatic CRC generation
- Wide RSSI (Received Signal Strength Indicator) dynamic range, 70dB from Rx noise floor
- Bit rates up to 200 kb/s, NRZ coding
- On-chip frequency synthesizer
- FSK and OOK modulation
- Incoming sync word recognition
- Built-in Bit-Synchronizer for incoming data and Clock synchronization and recovery

APPLICATIONS

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control

DEVICE OPTIONS

Part	Frequency band	Pin Package
DPS1211C868	868 - 870MHz	Board
DPS1211C915	902 - 928MHz	Board
DPS1211C950	950 - 960MHz	Board

Table of Contents

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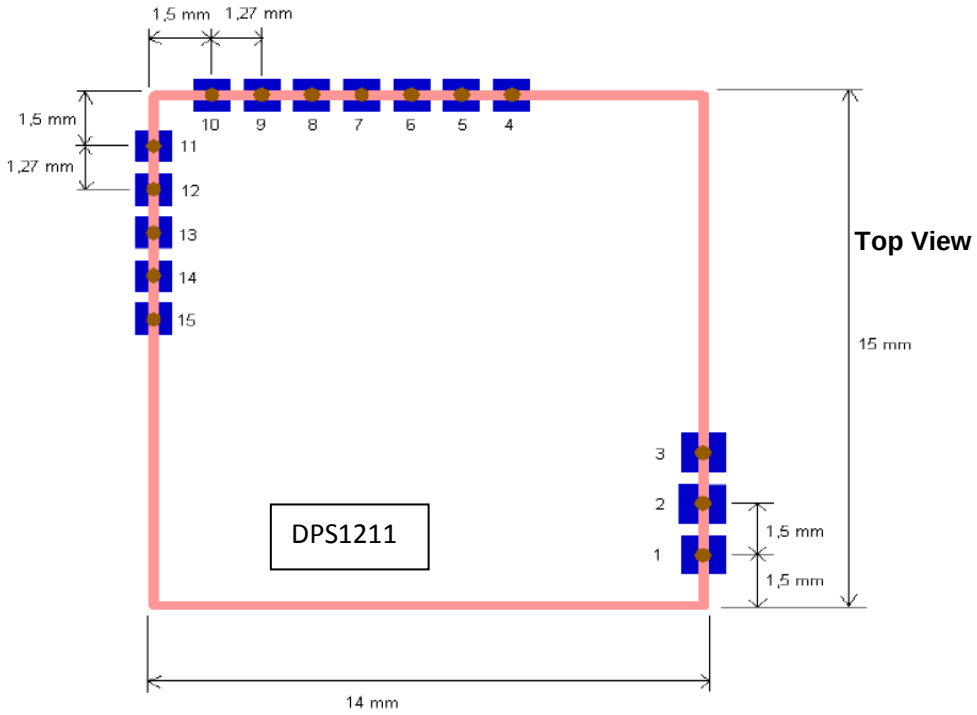
1. PIN DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	GND		Ground
2	RFIO	IN/OUT	RF Input / Output
3	GND		Ground
4	NSS_CONFIG	IN	SPI SELECT CONFIG
5	NSS_DATA	IN	SPI SELECT DATA / DATAIN
6	MISO	OUT	SPI Master Input Slave Output
7	MOSI	IN	SPI Master Output Slave Input
8	SCK	IN	SPI CLOCK
9	CLKOUT	OUT	Output clock at reference frequency divided by 2, 4, 8, 16, 32
10	DATA	IN/OUT	Data
11	IRQ0	OUT	Interrupt (PATTERN//FIFOEMPTY)
12	IRQ1	OUT	Interrupt(DCLK/FIFOFULL)
13	PLL_Lock	OUT	PLL lock detection Output
14	VCC		Supply Voltage
15	GND		Ground

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2. ELECTRICAL CHARACTERISTICS

2.1. ABSOLUTE MAXIMUM OPERATING RANGES

Description	Min	Max	Unit
Supply voltage	2.1	3.6	V
Operating temperature	-20	+70	°C
Storage temperature	-55	125	°C
Soldering temperature (max 15 sec)		260	°C

CAUTION: ESD sensitive device.
Precaution should be taken when handling the device in order to prevent permanent damage

Life Support Policy and Use in Safety Critical Applications

ANYLINK PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF ANYLINK PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE UNDERTAKEN SOLELY AT THE CUSTOMER'S OWN RISK.

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2.2. SPECIFICATIONS

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, carrier frequency = 869 or 915 MHz, modulation FSK, data rate = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FR	Synthesizer Frequency Range	DPS1211-C868 DPS1211-C915 DPS1211-C950	863 902 950	- - -	870 928 960	MHz MHz MHz
IDDSL	Sleep mode supply current		-	0.1	2	µA
IDDST	Standby mode supply current	12.8 MHz running	-	65	80	µA
IDDFS	Supply current in FS mode	Frequency synthesizer running		1.3	1.7	mA
IDDR	RX mode supply current			3	3.5	mA
IDDT	TX mode supply current	PRF = 1 dBm PRF = 10 dBm		16 25	21 30	mA mA
RFS_F	RF Sensitivity (FSK)* **	BR=25 kbps / 869 MHz BR=25 kbps / 915 MHz		-107 -105	- -	dBm dBm
RFS_O	RF Sensitivity (OOK)* **	BR=2 kbps / 869 MHz BR=2 kbps / 915 MHz		-113 -111	- -	dBm dBm
FDA	Frequency Deviation	Programmable	33	50	200	kHz
BR_F	Bit rate (FSK)	Programmable	1.56	-	200	kb/s
BR_O	Bit rate (OOK)		1.56	-	32	kb/s
RFOP	RF output power, programmable with 8 steps of typ. 3dB **	Programmable.	-8,5		+12,5	dBm
TS_TR	Transmitter wake-up time	From FS to Tx ready.	-	120	500	µs
TS_RE	Receiver wake up time	From FS to Rx ready.	-	280	500	µs
TS_OSC	Quartz oscillator wake up time	From sleep mode.	-	1.5	5	ms
XTAL	Quartz oscillator frequency			12.8		MHz

* All sensitivities are measured receiving a PN15 sequence, for a BER of 0.1%
** Insertion Loss of SAW Filter should be taken into account (about 2.8 dB for 868MHz Module)

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3. FUNCTIONAL DESCRIPTION

The DPS1211 is a cost effective high performance radio transceiver module designed for the wireless transmission of digital information.

The module is based on the RF transceiver circuit SX1211 from Semtech. For more information on the SX1211, please refer to the datasheet, available from the Semtech website:
http://www.semtech.com.

As illustrated below, illustrates the SX1211 data processing circuit. Its role is to interface the data to/from the modulator/demodulator and the µC access points (SPI, IRQ and DATA pins). It also controls all the configuration registers.

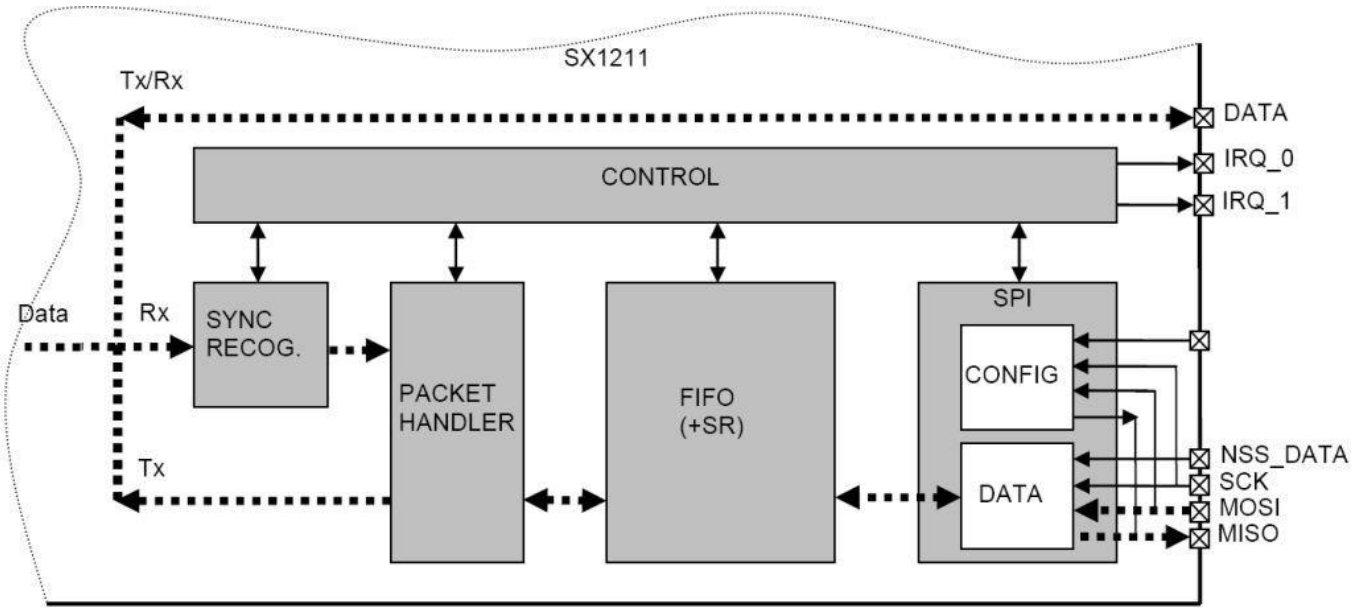

Figure 1

4. DATA OPERATION MODES

The DPS1211 has three different data operation modes selectable by the user:
Continuous mode: each bit transmitted or received is accessed in real time at the DATA pin. This mode may be used if adequate external signal processing is available.

Buffered mode: each byte transmitted or received is stored in a FIFO and accessed via the SPI bus. µC processing overhead is hence significantly reduced compared to Continuous mode operation. The packet length is unlimited.

Packet mode (recommended): user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically built with preamble, Sync word, and optional CRC, DC free encoding and the reverse operation is performed in reception. The µC processing overhead is hence reduced further compared to Buffered mode. The payload length is limited to 64 bytes (maximum FIFO size).

IRQParam_RX_stby_IRQ_0	MCParam_Data_Mode_0	IRQ_0_Rx	IRQ_0_Stby
00	00	Sync	In Continuous mode, no interrupt is available in Stby mode
01	00	RSSI	
10	00	Sync	
11	00	Sync	
00	01	-	-
01	01	Write_byte	-
10	01	/Fifoempty	/Fifoemtpy
11	01	Sync	-
00	1x	Payload_ready	-
01	1x	Write_byte	-
10	1x	/Fifoempty	/Fifoempty
11	1x	Sync or Adrs_match*	-

*The latter if Address filtering is enabled

Table 1: IRQ_0 interrupt sources in receive mode.

IRQParam_RX_stby_IRQ_1	MCParam_Data_Mode_0	IRQ_1_Rx	IRQ_1_Stby
00	00	DCLK	In Continuous mode, no interrupt is available in Stby mode
01	00		
10	00		
11	00		
00	01	-	-
01	01	Fifofull	Fifofull
10	01	RSSI	-
11	01	Fifo_threshold	Fifo_threshold
00	1x	CRC_OK	-
01	1x	Fifofull	Fifofull
10	1x	RSSI	-
11	1x	Fifo_threshold	Fifo_threshold

Table 2: IRQ_1 interrupt sources in receive mode.

For more information about the data operation modes, please refer to the SX1211 datasheet chapter: *Description* You can find this at http://www.semtech.com .

5. SERIAL CONTROL INTERFACE

SPI Config: used in all data operation modes to read and write the configuration registers which control all the Parameters of the chip (operating mode, bit rate, etc...)

SPI Data: used in Buffered and Packet mode to write and read data bytes to and from the FIFO. (FIFO Interrupts can be used to manage the FIFO content.)

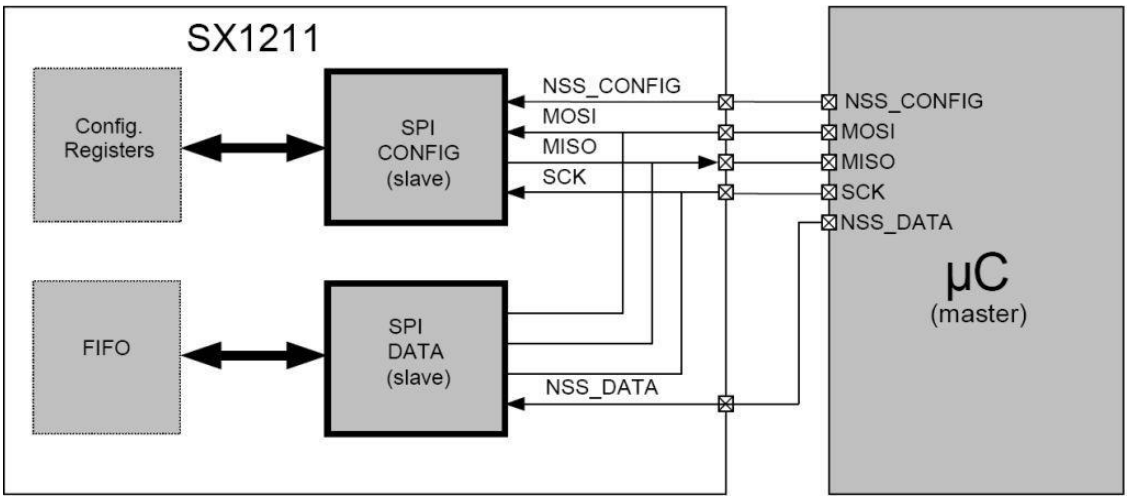

Figure 2, SPI Interface Overview and µC Connections

For more information about the serial interface, please refer to the SX1211 datasheet chapter: Serial Interface definition and principle of operation. You can find this on http://www.semtech.com .

6. PACKET MODE

6.1. GENERAL DESCRIPTION

In Packet mode the NRZ data to (from) the (de)modulator is not directly accessed by the µC but stored in the FIFO and accessed via the SPI Data Interface. In addition, the SX1211's packet handler performs several packet oriented tasks such as Preamble and Sync word generation, CRC calculation/check, whitening/dewhitening of data, address filtering, etc. This simplifies still further software and reduces µC overhead by performing these repetitive tasks within the RF chip itself.
Another important feature is ability to fill and empty the FIFO in Stby mode, ensuring optimum power consumption and adding more flexibility for the software.

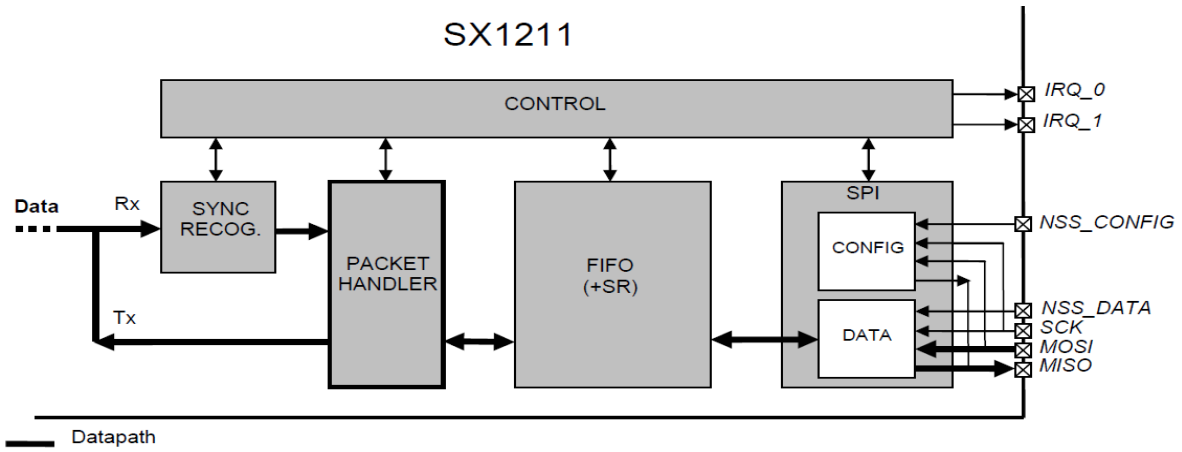

Figure 3, Packet Mode Conceptual View

Note that Bit Synchronizer and Sync word recognition are automatically enabled in Packet mode.

6.2. PACKET FORMAT

Two types of packet formats are supported: fixed length and variable length, selectable by the PKTParam_Pkt_format bit. The maximum size of the payload is limited by the size of the FIFO selected (16, 32, 48 or 64 bytes).

6.2.1. FIXED LENGTH PACKET FORMAT

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.
The length of the payload is set by the PKTParam_Payload_length register and is limited by the size of the FIFO selected.
The length stored in this register relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown in Figure 4. It contains the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Optional Address byte (Node ID).
- Message data.
- Optional 2-bytes CRC checksum.

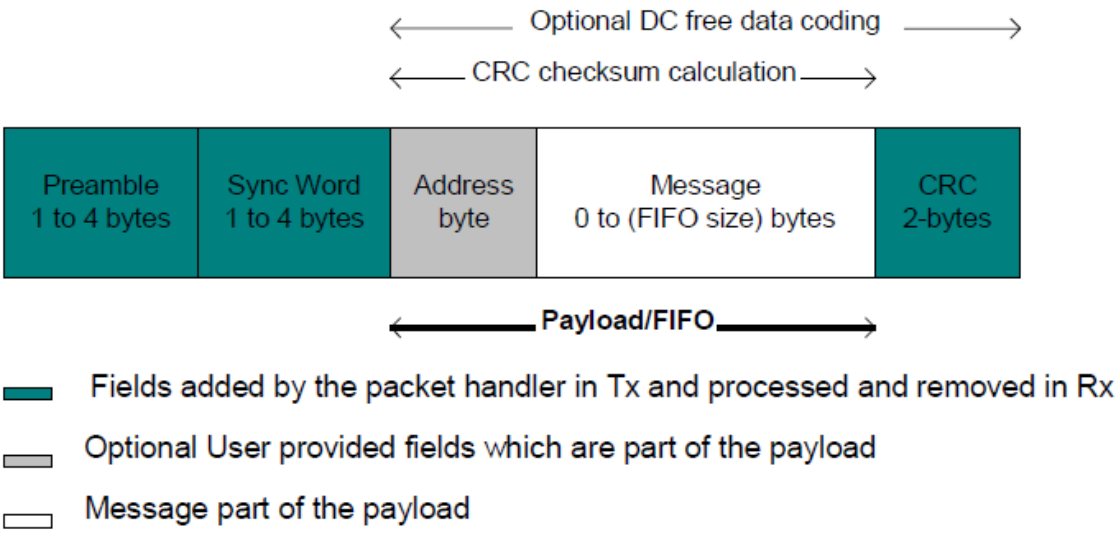

Figure 4, Fixed Length Packet Format

For more information about the modes of operation, please refer to the SX1211 Datasheet on the Semtech website http://www.semtech.com .

6.2.2. VARIABLE LENGTH PACKET FORMAT

This mode is necessary in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.
In this mode the length of the payload, indicated by the length byte in Figure 5, is given by the first byte of the FIFO and is limited only by the width of the FIFO selected. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown in Figure 5. It contains the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Length byte
- Optional Address byte (Node ID).
- Message data.
- Optional 2-bytes CRC checksum.

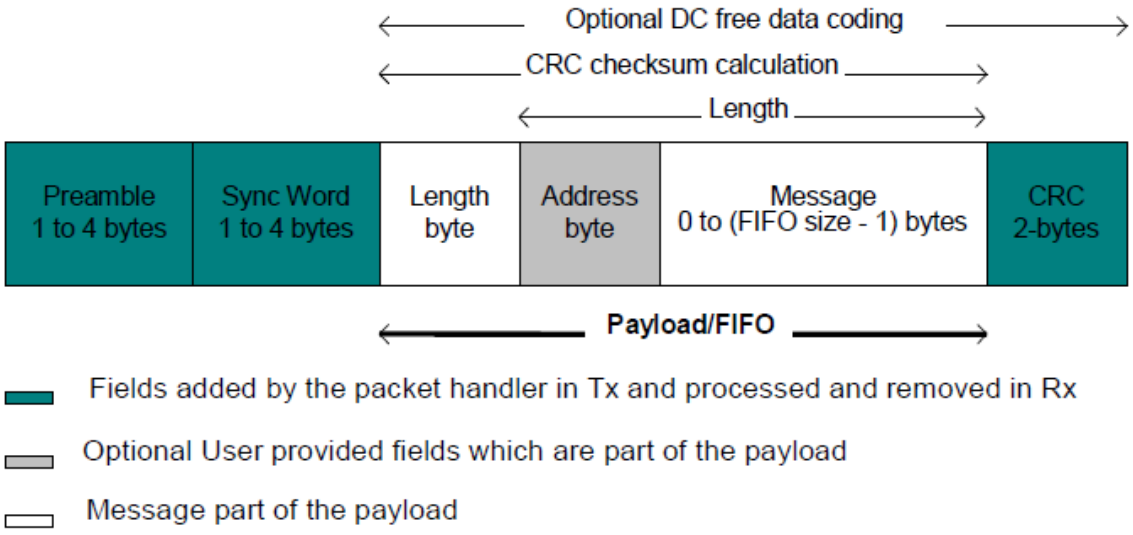

Figure 5, Variable Length Packet Format

For more information about the modes of operation, please refer to the SX1211 Datasheet on the Semtech website http://www.semtech.com .

7. MECHANICAL DIMENSIONS

The following diagram shows the physical footprint and dimensions of the DPS1211 drop-in module.

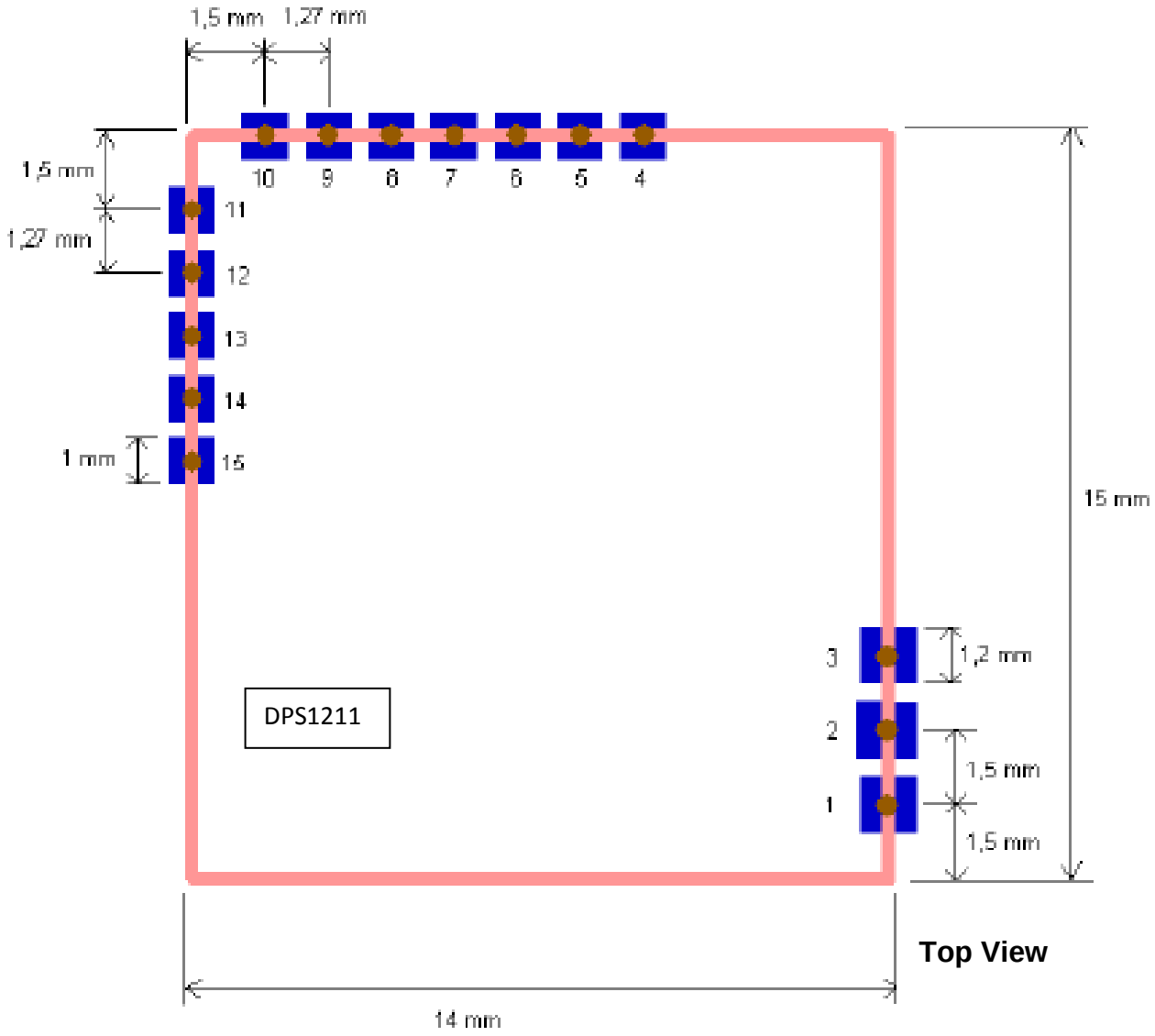

Figure 6

Version	Create Date:	Creater	Changes
01	25.10.2012	Goldmann	Release Preliminary Datasheet
02	04.11.2016	H.M.	Temp. Range

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