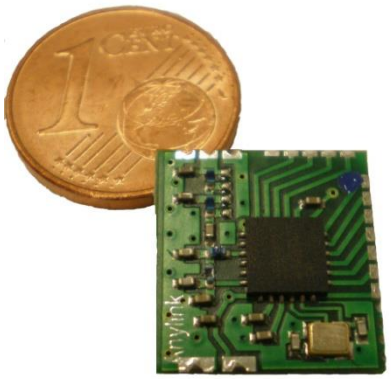

DP1231 – C315/C433/C868/C915

315, 433, 868 and 915 MHz Drop-In RF Transceiver Modules

Combine Small Form Factor with High Performance

GENERAL DESCRIPTION

The DP1231 is a low cost transceiver module operating in the frequency ranges from 290-340 MHz, 424-510, 862- 1020 MHz. The DP1231 is optimized for High Link Budget and for very small form factor. It incorporates a baseband modem with data rates up to 300 kb/s. Data handling features include a 66 byte FIFO, packet handling, automatic CRC generation and data whitening. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC part 15) regulatory standards.

KEY PRODUCT FEATURES

- Low area needed
- FSK and OOK modulation
- Constant Output power from 1.8 to 3.6 Volt
- Good reception sensitivity: down to -120 dBm at 1.2 kb/s in FSK, -112 dBm at 4.8kb/s in OOK
- Programmable RF output power: up to +13 dBm in 1 dB steps starting from -18 dBm
- Packet handling feature with data whitening and automatic CRC generation
- RSSI (Received Signal Strength Indicator) range from noise floor to 0 dBm
- Bit rates up to 300 kb/s, NRZ coding
- On-chip frequency synthesizer
- Incoming sync word recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery

APPLICATIONS

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control

DEVICE OPTIONS

Part	Frequency band	Pin Package
DP1231C315	290 - 340 MHz	Board
DP1231C433	424 - 510 MHz	Board
DP1231C868	862 - 902 MHz	Board
DP1231C915	902 - 1020 MHz	Board

Table of Contents

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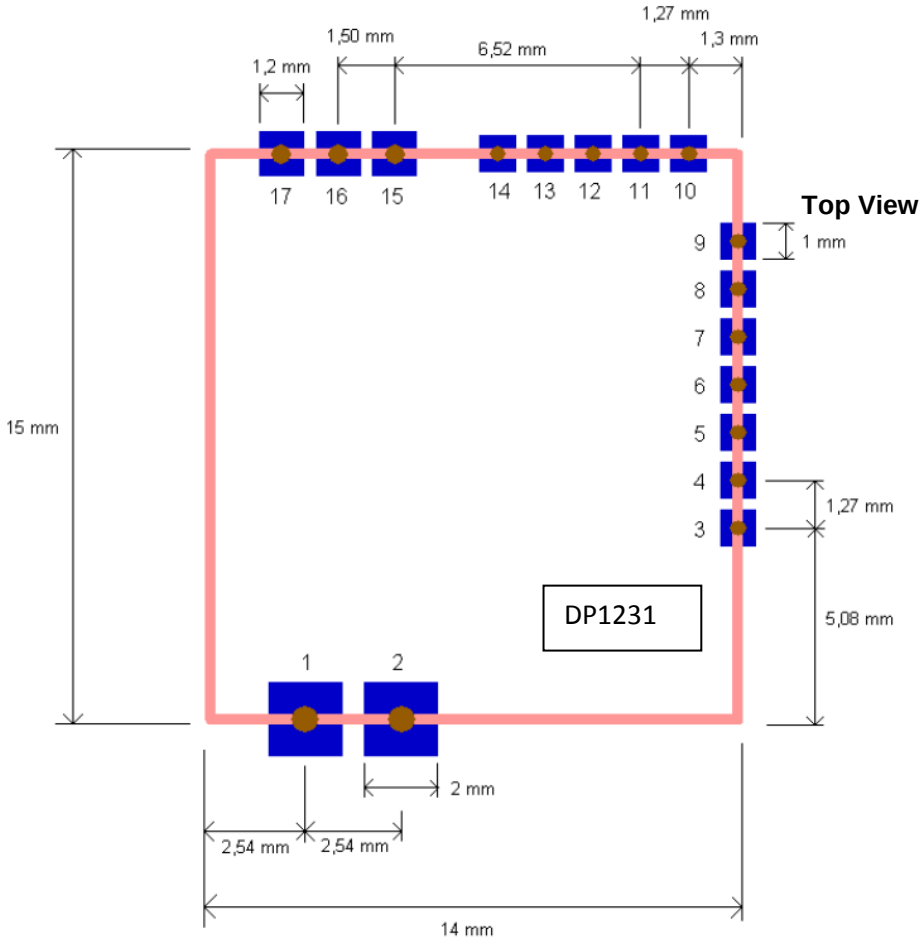
1. PIN DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	GND		Ground
2	VCC		Supply Voltage
3	RESET	IN/OUT	Reset trigger input
4	DIO0	IN/OUT	Digital I/O, software configured
5	DIO1/DCLK	IN/OUT	Digital I/O, software configured
6	DIO2/DATA	IN/OUT	Digital I/O, software configured
7	DIO3	IN/OUT	Digital I/O, software configured
8	DIO4	IN/OUT	Digital I/O, software configured
9	DIO5	IN/OUT	Digital I/O, software configured
10	SCK	IN	SPI Clock input
11	MISO	OUT	SPI Data output
12	MOSI	IN	SPI Data input
13	NSS	IN	SPI Chip select input
14	RXTX	OUT	Rx/Tx switch control: high in Tx – Mode
15	GND		Ground
16	RF_IN_OUT	IN/OUT	RF Input / Output terminal
17	GND		Ground

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2. ELECTRICAL CHARACTERISTICS

2.1. ABSOLUTE MAXIMUM OPERATING RANGES

Description	Min	Max	Unit
Supply voltage	1.8	3.6	V
Operating temperature	-20	+70	°C
Storage temperature	-55	125	°C
Soldering temperature (max 15 sec)		260	°C

CAUTION: ESD sensitive device.
Precaution should be taken when handling the device in order to prevent permanent damage

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2.2. SPECIFICATIONS

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VDD=3.3 V, temperature = 25 °C, *FXOSC* = 32 MHz, *F*RF = 915 MHz, Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FR	Synthesizer Frequency Range	DP1231-C315	290	-	340	MHz
		DP1231-C433	424	-	510	MHz
		DP1231-C868	862	-	902	MHz
		DP1231-C915	902	-	1020	MHz
IDDSL	Supply current in Sleep mode		-	0.1	1	µA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	µA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.25	1.5	mA
IDDFS	Supply current in Synthesizer mode		-	9	-	mA
IDDR	RX mode supply current		-	16	-	mA
IDDT	TX mode supply current	RFOP = +13 dBm	-	45	-	mA
		RFOP = +10 dBm	-	33	-	mA
		RFOP = 0 dBm	-	20	-	mA
		RFOP = -1 dBm	-	16	-	mA
RFS_F	RF Sensitivity (FSK)	FDA=5kHz, BR = 1.2kb/s*	-	-120	-	dBm
		FDA=5kHz, BR = 4.8kb/s	-	-114	-	dBm
		FDA=40kHz,BR=38.4kb/s	-	-105	-	dBm
RFS_O	RF Sensitivity (OOK)	BR = 4.8 kb/s	-	-112	-109	dBm
FDA	Frequency Deviation	Programmable FDA + BRF/2=<500kHz	0.6	-	300	kHz
BR_F	Bit rate (FSK)	Programmable	1.2	-	300	kb/s
BR_O	Bit rate (OOK)	Programmable	1.2	-	32.768	kb/s
RFOP	RF output power, programmable in 1dB steps	Programmable.	-18		+13	dBm
TS_TR	Transmitter wake-up time, to the first rising edge of DCLK	Frequency Synthesizer on, PaRamp=10µs,BR=4.8kb/s	-	120	-	µs
TS_RE	Receiver wake up time, from PLL locked state to *RXReady*	RxBw=10kHz,BR=4.8kb/s	-	1.7	-	Ms
		RxBw=200kHz,BR=100kb/s	-	96	-	µs
TS_OSC	Quartz oscillator wake up time		-	250	500	µs
XTAL	Quartz oscillator frequency			32		MHz

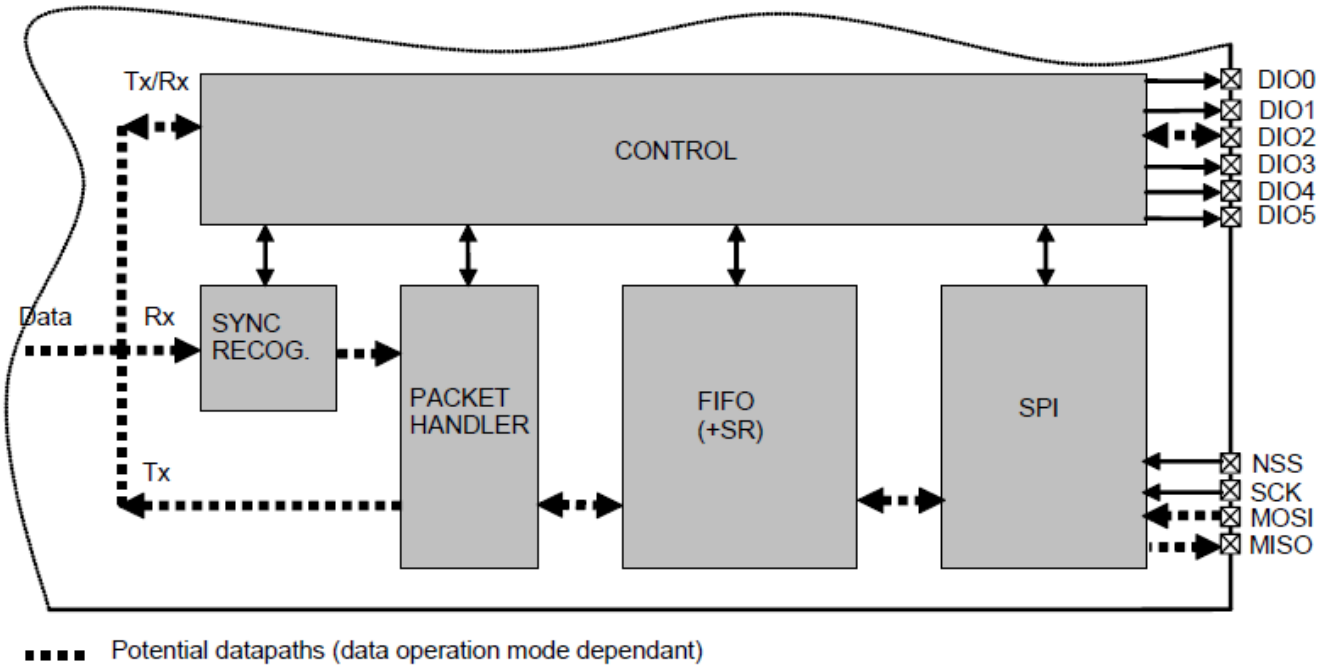
**Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver*

3. FUNCTIONAL DESCRIPTION

The DP1231 is a cost effective high performance radio transceiver module designed for the wireless transmission of digital information.

The module is based on the RF transceiver circuit from Semtech, the SX1231. For more information on the SX1231, please refer to the datasheet, available from the Semtech website:
http://www.semtech.com .

Figure below illustrates the SX1231 data processing circuit. Its role is to interface the data to/from the modulator/ demodulator and the uC access points (SPI and DIO pins). It also controls all the configuration registers.



4. DATA OPERATION MODES

The DP1231 has two different data operation modes selectable by the user:

Continuous mode: each bit transmitted or received is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.

Packet mode (recommended): user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically
built with preamble, Sync word, and optional AES, CRC, and DC-free encoding schemes The reverse operation is performed in reception. The uC processing overhead is hence significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, AES, etc) the maximum payload length is limited to FIFO size, 255 bytes or unlimited.

For more information about the data operation modes, please refer to the SX1231 datasheet chapter: *Description*. You can find this at http://www.semtech.com .

5. Digital IO Pins Mapping

Six general purpose IO pins are available on the SX1231, and their configuration in Continuous or Packet mode is controlled through *RegDioMapping1* and *RegDioMapping2.*

5.1 DIO Pins Mapping in Continuous Mode

Mode	Diox Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
Sleep	00	-	-	-	-	-	-
	01	-	-	-	-	-	-
	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	-	-	-	-	ModeReady
Stdby	00	ClkOut	-	-	-	-	-
	01	-	-	-	-	-	-
	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	-	-	-	-	ModeReady
FS	00	ClkOut	-	-	-	-	PllLock
	01	-	-	-	-	-	-
	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	PllLock	-	-	PllLock	ModeReady
Rx	00	ClkOut	Timeout	Rssi	Data	Dclk	SyncAddress
	01	Rssi	RxReady	RxReady	Data	RxReady	Timeout
	10	LowBat	SyncAddress	AutoMode	Data	LowBat	Rssi
	11	ModeReady	PllLock	Timeout	Data	SyncAddress	ModeReady
Tx	00	ClkOut	TxReady	TxReady	Data	Dclk	PllLock
	01	ClkOut	TxReady	TxReady	Data	TxReady	TxReady
	10	LowBat	LowBat	AutoMode	Data	LowBat	LowBat
	11	ModeReady	PllLock	TxReady	Data	PllLock	ModeReady

5.2 DIO Pins Mapping in Packet Mode

Mode	Diox Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
Sleep	00	-	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
Stdby	00	ClkOut	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
FS	00	ClkOut	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PllLock	PllLock	AutoMode	PllLock	PllLock
Rx	00	ClkOut	Timeout	FifoFull	FifoNotEmpty	FifoLevel	CrcOk
	01	Data	Rssi	Rssi	Data	FifoFull	PayloadReady
	10	LowBat	RxReady	SyncAddress	LowBat	FifoNotEmpty	SyncAddress
	11	ModeReady	PllLock	PllLock	AutoMode	Timeout	Rssi
Tx	00	ClkOut	ModeReady	FifoFull	FifoNotEmpty	FifoLevel	PacketSent
	01	Data	TxReady	TxReady	Data	FifoFull	TxReady
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PllLock	PllLock	AutoMode	PllLock	PllLock

For more information about the data operation modes, please refer to the SX1231 datasheet chapter: *Description*. You can find this on http://www.semtech.com .

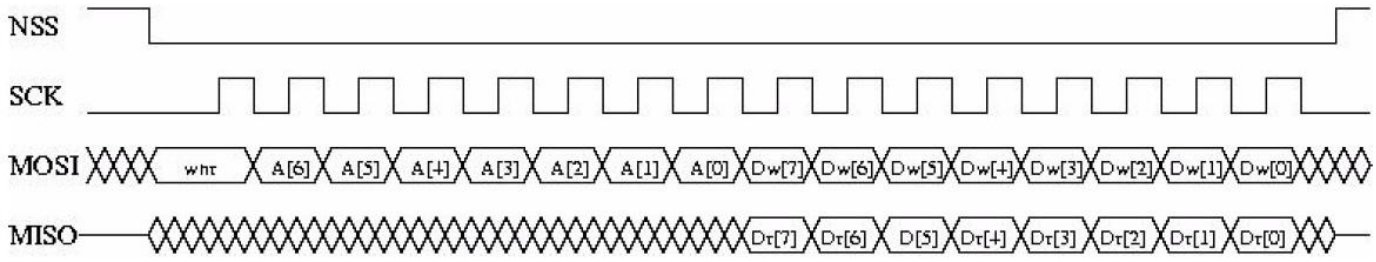
6. SPI Interface description

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL= 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the begin of the frame and goes high after the data byte.
- BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- FIFO access: if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

Figure below shows a typical SPI single access to a register.



MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.
A transfer always starts by the NSS pin going low. MISO is high impedance when NSS is high.

For more information about the serial interface, please refer to the SX1231 datasheet chapter: *Control Block Description.* You can find this at http://www.semtech.com .

7. OPERATING MODES

The circuit can be set in 5 different basic modes which are described in Table 14.

By default, when switching from a mode to another one, the sub-blocks are woken up according to a pre-defined and optimized sequence. Alternatively, these operating modes can be selected directly by disabling the automatic sequencer (*SequencerOff* in *RegOpMode = 1*).

ListenOn in RegOpMode	Mode in RegOpMode	Selected Mode	Enabled blocks
0	000	Sleep Mode	None
0	001	Stand-by Mode	Top regulator and crystal oscilator
0	010	FS Mode	Frequency synthesizer
0	011	Transmit Mode	Frequency synthesizer and transmitter
0	100	Receive Mode	Frequency synthesizer and receiver
1	x	Listen Mode	See Liste Mode (7.1)

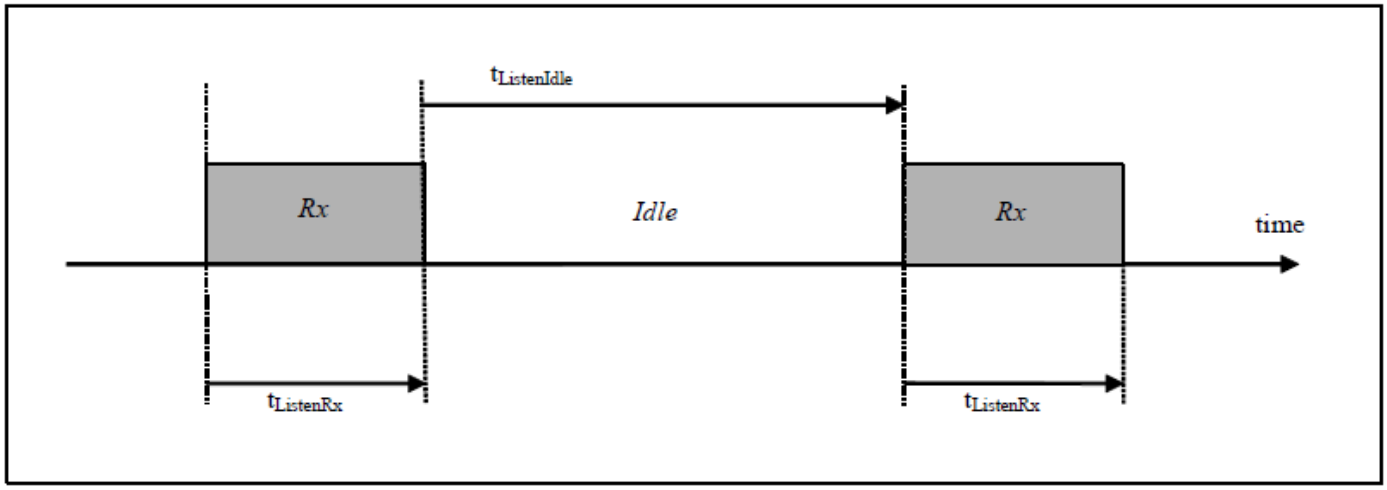
7.1 Listen Mode

The circuit can be set to Listen mode, by setting *ListenOn* in *RegOpMode* to 1. In this mode, SX1231 spends most of the time in Idle mode, during which only the RC oscillator runs. Periodically the receiver is woken up and listens for an RF signal. If a wanted signal is detected, the receiver is kept on and the data is demodulated.

Otherwise, if a wanted signal hasn't been detected after a pre-defined period of time, the receiver is disabled until the next time period.

This periodical Rx wake-up requirement is very common in low power applications. On SX1231 it is handled locally by the Listen mode block without using uC resources or energy.

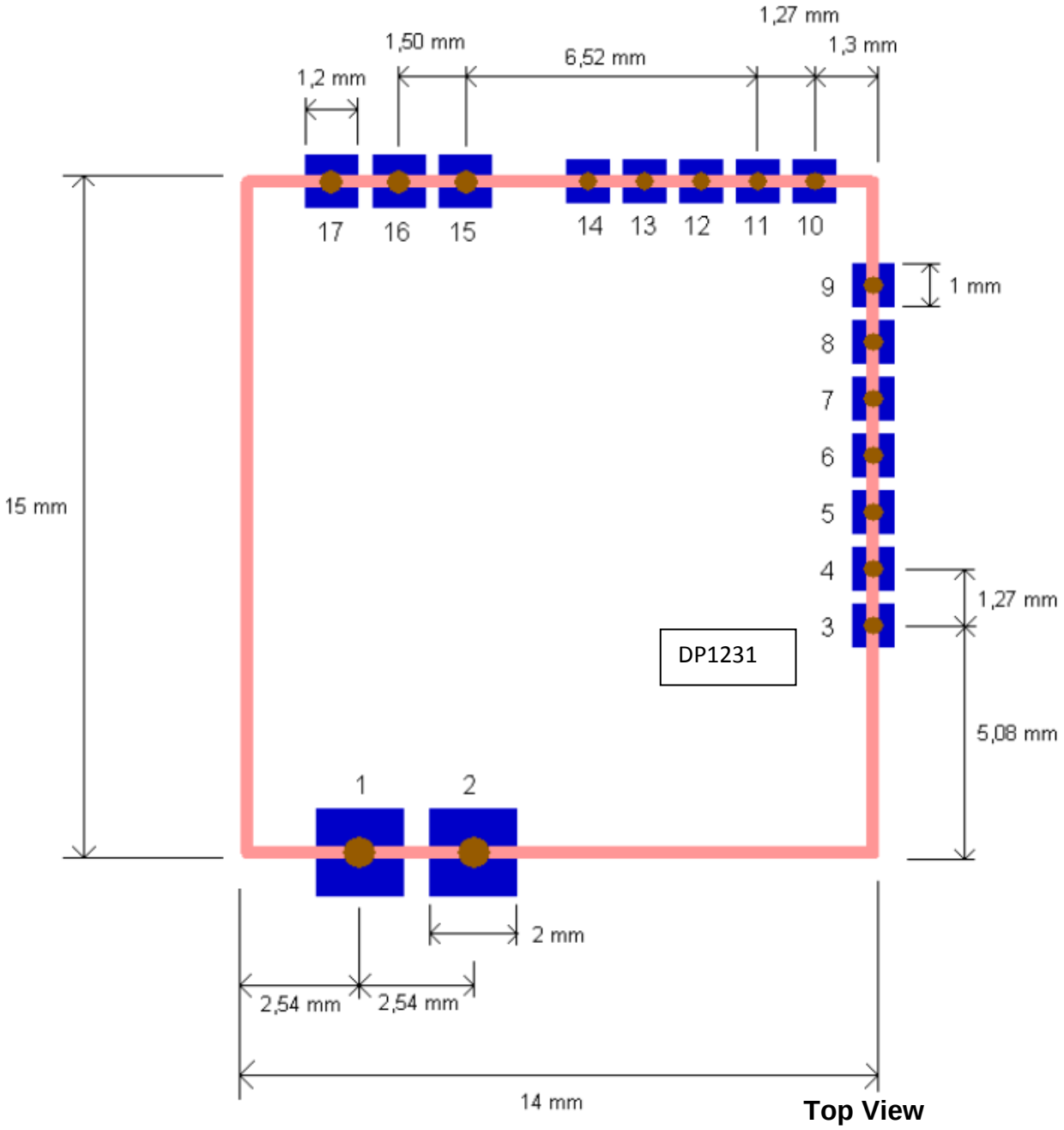
The simplified timing diagram of this procedure is illustrated in Figure 19.



For more information about the modes of operation, please refer to the SX1231 Datasheet on the Semtech website http://www.semtech.com .

8. MECHANICAL DIMENSIONS

The following drawing shows the physical footprint and dimensions of the DP1231 drop-in module.



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Version	Create Date:	Creater	Changes
01 preliminary	13.02.12	Hermann	Create new Datasheet
02 preliminary	01.06.12	Hermann	Add Information
03	04.11.16	H.M.	Temp. Range

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